Abstract of the Disclosure

Disclosed is a method and apparatus for providing a universal SCSI bus interface in which bus performance is not degraded, and the analyzer is not negatively influenced by post processing while maintaining the ability to filter and store data using any of a number of generic logic analyzers. The SCSI bus interface does not rely on a specific clock speed and maintains the ability to view both raw data and protocol errors. The universal SCSI bus interface embodiments described herein produce stable clock signals for use by an analyzer in a form that is phase and frequency stabilized with the SCSI bus clock. This allows data sampling to mimic the performance characteristics of a device attached to the SCSI bus thereby minimizing sampling error.